AMENDMENTS TO THE CLAIMS

1. (Original) A method of producing a carrier wafer for an integrated circuit, said method comprising the steps of:

providing a carrier wafer having a plurality of bump pads and a plurality of wire bond pads;

providing a passivation layer on said carrier wafer;

etching a passivation layer over at least a portion of said plurality of bump pads;

applying solder bumps on said plurality of bump pads; and

separately etching the passivation layer over at least a portion of said plurality of wire bond pads.

2. (Original) The method of claim 1 wherein said step of providing a carrier wafer comprises a step of providing a carrier wafer having traces connecting at least a portion of said plurality of bump pads.

3. (Original) The method of claim 2 further comprising a step of coupling a flip chip to said carrier wafer.

4. (Original) The method of claim 3 wherein said step of coupling said flip chip to said carrier wafer comprises a step of coupling said flip chip to another flip chip by way of said traces on said substrate.

5. (Original) The method of claim 1 further comprising a step of providing wire bonds between said plurality of wire bond pads and a plurality of wire bond pads on a substrate.

6. (Original) A method of producing a carrier wafer for an integrated circuit, said method comprising the steps of:

providing a passivation layer over a plurality of bump pads and a plurality of wire bond pads formed on a carrier wafer;

etching said passivation layer over at least a portion of said plurality of bump pads;

applying solder bumps on said plurality of bump pads;

separately etching the passivation layer over at least a portion of said plurality of said wire bond pads; and

coupling a flip chip to said plurality of bump pads.

7. (Original) The method of claim 6 further comprising a step of providing traces connecting at least some of said plurality of bump pads on said carrier wafer.

8. (Original) The method of claim 7 wherein said step of coupling a flip chip to said plurality of bump pads comprises a step of coupling said flip chip to another flip chip by way of said traces.

9. (Original) The method of claim 8 further comprising a step of connecting programmable logic of said flip chip to programmable logic of said other flip chip.

10. (Original) The method of claim 6 further comprising a step of providing a wire bond between said plurality of wire bond pads and a plurality of wire bond pads on a substrate.

11. (Original) A method of producing a carrier wafer for an integrated circuit, said method comprising the steps of:

providing a silicon carrier wafer having a plurality of bump pads connected by a plurality of traces, and a plurality of wire bond pads;

providing a passivation layer over said plurality of bump pads and said plurality of wire bond pads;

etching said passivation layer over said plurality of bump pads;

applying solder bumps on said plurality of bump pads;

separately electing said passivation layer over said plurality of wire bond pads; and

coupling a plurality of flip chips to said plurality of bump pads.

12. (Original) The method of claim 11 comprising a step of connecting a region of a first flip chip to a region of a second flip chip.

13. (Original) The method of claim 12 wherein said step of connecting a region of a first flip chip to a region of a second flip chip comprises a step of connecting programmable logic of said first flip chip and said second flip chip.

14. (Original) The method of claim 11 further comprising a step of providing a wire bond between a wire bond pad of said plurality of wire bond pads and a wire bond pad of a substrate.

15. (Original) A method of producing a carrier wafer for an integrated circuit, said method comprising the steps of:

providing a silicon carrier wafer having a plurality of bump pads connected by a plurality of traces and a plurality of wire bond pads;

providing a passivation layer on said plurality of bump pads and said plurality of wire bond pads;

etching said plurality of bump pads;

applying solder bumps on said plurality of bump pads;

separately electing said passivation layer over said plurality of wire bond pads after applying said solder bumps;

positioning a plurality of flip chips on said plurality of bump pads;

coupling said carrier wafer to a substrate;

providing a plurality of wire bonds between said plurality of wire bond pads and a plurality of wire bond pads on said substrate;

applying an encapsulation layer over said flip chips and said plurality of wire bonds;

applying a plurality of solder balls to said substrate; and

attaching a metal lid over said substrate.

Claims 16-25 (Cancelled)